CLAIMS

What is claimed is:

1. A method comprising:

disposing a trench layer upon a semiconductor substrate;

selectively removing a portion of the trench layer such that a remainder of the trench layer forms one or more trenches, the removal of a portion of the trench layer exposing the semiconductor substrate;

filling the one or more trenches with a semiconductor material;

removing any excess semiconductor material from the one or more trenches; and

removing an additional portion of the trench layer to expose the semiconductor material as one or more semiconductor fins.

2. The method of claim 1 wherein the trench layer is comprised of a plurality of layers.

3. The method of claim 2 wherein the plurality of layers include a first oxide layer disposed upon the semiconductor substrate, a nitride layer disposed upon the first oxide layer, and a second oxide layer disposed upon the nitride layer.

4. The method of claim 3 wherein removing an additional portion of the trench layer comprises removing any remaining portion of the second oxide layer, any remaining portion of the nitride layer, and retaining at least some portion of any remaining portion of the first oxide layer.

5. The method of claim 1 wherein the one or more trenches have a depth of approximately 10 nm.

6. The method of claim 5 wherein the one or more semiconductor fins have a height of approximately 10 nm that is uniform to within 5%.

7. The method of claim 1 wherein removing any excess semiconductor material from the one or more trenches includes planarizing the semiconductor material to a surface of the trench layer.

8. The method of claim 7 wherein the planarizing is effected through a chemical-mechanical polishing process.

9. The method of claim 1 wherein filling the one or more trenches with a semiconductor material includes epitaxially growing the semiconductor material within the one or more trenches.

10. The method of claim 1 wherein filling the one or more trenches with a semiconductor material includes a blanket deposition of semiconductor material.

11. An integrated circuit device comprising:

a substrate; and

one or more transistors formed upon the substrate, each transistor having a semiconductor body, each semiconductor body having a height of less than 20 nm, the height of each semiconductor body uniform to within a tolerance of 5% of a specified height.

12. The integrated circuit device of claim 11 wherein the one or more transistors are tri-gate transistors.

13. The integrated circuit device of claim 12 wherein each semiconductor body has a height of approximately 10 nm.

14. A method comprising:

disposing a first oxide layer on a semiconductor substrate;

disposing a nitride layer upon the first oxide layer;

disposing a second oxide layer upon the nitride layer;

selectively etching a portion of the second oxide layer and the nitride layer to define one or more trenches;

filling the one or more trenches with a semiconductor material;

removing the excess semiconductor material from the one or more trenches; and

selectively etching a remainder of the second oxide layer and the nitride layer such that one or more semiconductor bodies are formed.

15. The method of claim 14 wherein the one or more trenches have a depth of approximately 10 nm.

16. The method of claim 14 wherein the one or more semiconductor bodies have a height of less than 20 nm that is uniform to within 5%.

17. The method of claim 16 wherein the one or more semiconductor bodies have a height of approximately 10 nm.

18. The method of claim 14 wherein removing any excess semiconductor material from the one or more trenches includes planarizing the semiconductor material to a surface of the second oxide layer.

19. The method of claim 18 wherein the planarizing is effected through a chemical-mechanical polishing process.

20. The method of claim 14 wherein filling the one or more trenches with a semiconductor material includes epitaxially growing the semiconductor material within the one or more trenches.

21. The method of claim 14 wherein filling the one or more trenches with a semiconductor material includes a blanket deposition of semiconductor material.

22. The method of claim 14 wherein the semiconductor substrate is comprised of a semiconductor material selected from the group consisting of silicon, germanium, and gallium arsenide.

23. The method of claim 14 wherein the semiconductor substrate is comprised of silicon, the first oxide layer is comprised of SiO_2, the nitride layer is comprised of Si_3N_4, and the second oxide layer is comprised of SiO_2.